

Compensation of Non-Linearities in Diode-Clamped Multilevel Converters

Stephen R. Minshull, Christopher M. Bingham, *Member, IEEE*, David A. Stone, and Martin. P. Foster

Abstract—The application of multilevel converters for exciting permanent magnet machines with low-phase inductance to DC-link voltage ratios facilitates a reduction in high frequency switching harmonics. However, converter non-linearities and, in particular, on-state device voltage drops, create additional low-frequency harmonics. This paper therefore proposes a generic compensation scheme to accommodate the effects of such converter non-linearities and, in so doing, improve the harmonic quality of the machine phase currents. Experimental results gathered from a prototype 5-level diode clamped converter validate the benefits of the proposed scheme by showing quantitative reductions in low frequency harmonics.

Index Terms—Dead-time compensation, multilevel converter, permanent magnet synchronous motor, space vector modulation.

I. INTRODUCTION

MULTILEVEL inverters are an attractive choice for driving high-efficiency brushless permanent-magnet machines (with either sinusoidal or trapezoidal back-emf) that exhibit low phase inductance due to their high fundamental electrical frequency or those that require the series connection of power devices to provide adequate breakdown characteristics. Such inverters allow a reduction in the current ripple on the machine phase currents without an increase in the inverter switching frequency. Reduced current ripple also has associated benefits for torque ripple, eddy current machine losses and electromagnetic interference (EMI) [1, 2].

However, multilevel inverters, like their classical 2-level counterparts, are subject to the non-linear characteristics of their constituent switching devices. Finite switching times dictate that a blanking-time be inserted between one device being turned off in a phase leg and the complementary device being turned on to prevent a short-circuit, or “shoot-through” condition, forming across the inverter voltage source. However, the blanking-time introduces a voltage error at the converter phase terminals that is dependent on the phase current polarity. The effects and compensation of this

blanking-time have been well documented for 2-level converters [3-7] and also considered for a 3-level Neutral Point Clamped (NPC) converter [8]. These methods can be divided into schemes that achieve compensation by modifying the commanded converter terminal voltages [4, 5, 8] or pulse-based methods which directly modify the lengths of the gate-drive pulses in the modulator [4, 6, 7].

Other inverter non-linearities such as switching device on-state voltages and device turn on/off times have also been considered in addition to the blanking-time, and their combined impact is often termed “dead-time” effects. For 2-level inverters, such dead-time effects have been considered and compensation schemes have been previously reported that adjust the commanded converter terminal voltages accordingly [9-15]. The cycle-by-cycle amount of compensation to be added to the converter terminal voltages depends upon parameters that are often difficult to measure, and typically vary over the operating range of the converter. For this reason, disturbance observers [12, 15], self-commissioning schemes [13] and model reference adaptive systems (MRAS) [14] have also been utilised to increase the accuracy of the dead-time compensation for 2-level converter counterparts, with varying degrees of success.

For multilevel inverters applied to the excitation of machines that exhibit low-phase inductance vs. DC-link voltage ratios, such non-linearities in the converter phase voltages becomes readily apparent as low frequency harmonics in the phase currents. Moreover, the control of multilevel converters has an additional degree of freedom in the choice between redundant switching vectors that produce identical line-line terminal voltages, which is not present in traditional 2-level counterparts. As will be shown, the choice of these redundant vectors affects the dead-time compensation requirement with the compensation value depending on the particular switching vector chosen for a modulation cycle. In addition, the on-state voltage drops are increased due to the series connection of switching devices, when compared to classical 2-level converters.

This paper therefore addresses the compensation of dead-time effects for multilevel converters, complicated by the requirements of redundant vector application, by utilizing a combination of converter terminal voltage modification and pulse-based methods. It is highlighted that the application of redundant vectors, for the multilevel case, makes the use of previously reported adaptive schemes, for 2-level converters,

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difficult. Nevertheless, this work ‘opens the door’ for further development in this area.

The presented techniques are implemented on a prototype 5-level, back-to-back connected, Diode-Clamped Converter (DCC). However, it should be noted that the underlying principles presented are generic and more widely applicable to other multilevel topologies with any number of levels.

II. INVERTER TERMINAL VOLTAGE DETERMINATION

Fig. 1 shows a schematic of a single leg of a DCC connected to the multilevel DC-link that is common to all legs. The IGBT switching devices are shown as Q1-Q8 in Fig.1. D1-D8 are freewheel diodes while D9-D14 are added to clamp the output voltage to one of the multilevel DC-link voltages formed across C1-C4. The high-side switches form complementary pairs with the low-side switches. For example, Q1 switches in anti-phase with Q5, Q2 switches in anti-phase to Q6, and so on. Table 1 shows the desired phase terminal voltages, V_{AN} , the gate drive requirements for Q1-Q8, and the actual phase terminal voltages produced for current flowing from the leg, into the load, $V_{AN}, I_{ph} > 0$, and current flowing from the load, into the leg, $V_{AN}, I_{ph} < 0$. For the gate drive values, “1” indicates the IGBT is turned on and “0” indicates the IGBT is off. It can be seen from Table 1 that an error exists between the commanded phase voltages and those produced at the converter leg and that this error is dependent upon the current polarity. The error is due to the on-state voltage drops across the conducting devices, viz: IGBT (V_{CEon}), the freewheel diodes (V_{ff}) and the clamping diodes (V_{fc}). By way of example, referring to Fig.1, a demanded phase voltage of $V_{dc}/2$ with positive current creates a current path through D12, Q3 and Q4 resulting in the phase terminal voltage being: $V_{dc}/2 - 2V_{CEon} - V_{fc}$. A negative current for the same demanded voltage dictates a current path through Q5, Q6 and D11 resulting the phase terminal voltage of: $V_{dc}/2 + 2V_{CEon} + V_{fc}$.

TABLE I
IDEAL PHASE VOLTAGES, IGBT GATE VALUES AND ACTUAL PHASE TERMINAL VOLTAGES

V_{AN}	Q1-Q8	$V_{AN}, I_{ph} > 0$	$V_{AN}, I_{ph} < 0$
0	00001111	$0 - 4V_{ff}$	$0 + 4V_{CEon}$
$V_{dc}/4$	00011110	$V_{dc}/4 - V_{CEon} - V_{fc}$	$V_{dc}/4 + 3V_{CEon} + V_{fc}$
$V_{dc}/2$	00111100	$V_{dc}/2 - 2V_{CEon} - V_{fc}$	$V_{dc}/2 + 2V_{CEon} + V_{fc}$
$3V_{dc}/4$	01111000	$3V_{dc}/4 - 3V_{CEon} - V_{fc}$	$3V_{dc}/4 + V_{CEon} + V_{fc}$
V_{dc}	11110000	$V_{dc} - 4V_{CEon}$	$V_{dc} + 4V_{ff}$

For a 3-phase system, the actual phase voltages can be transformed into a stationary, orthogonal, $\alpha\beta$ reference frame using:

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

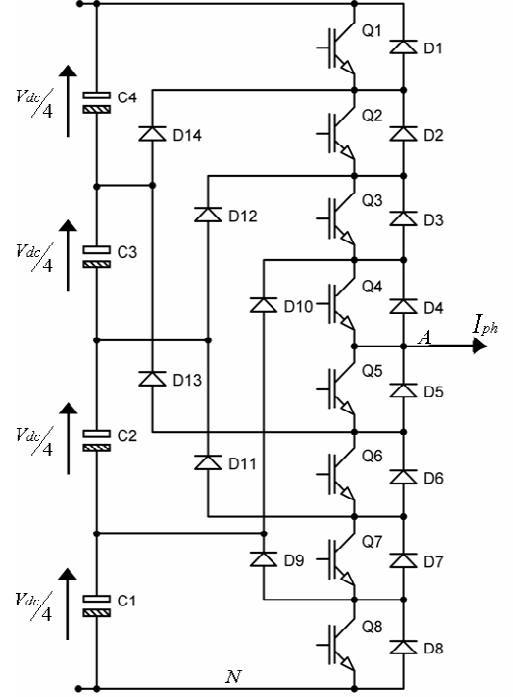


Fig. 1. Single leg of 5-level DCC connected to multilevel DC-link.

A space-vector (SV) diagram for realising space vector modulation (SVM) of the 5-level converter, can then be formed. SVM is employed for the modulation of the back-to-back DCC since it readily lends itself to implementation in regularly sampled digital control systems, and provides a means of balancing the series connected DC-link capacitors with the application of redundant vectors.

Each switching vector can take 1 of 6 possible values corresponding to the 6 possible 3-phase current polarities. For convenience it is necessary to consider only the first sector of the SV diagram since the remaining 5 sectors can be formed by use of transform tables [16]. The first sector of the 5-level SV diagram is shown in Fig. 2 with the parameters: $V_{dc} = 220V$, $V_{CEon} = 2.0V$, $V_{ff} = 1.8V$ and $V_{fc} = 0.8V$.

It can be seen from Fig.2 that there exists an appreciable error between the ideal vector locations and the actual locations when the voltage drops across the conducting devices are included. If ideal vector positions are assumed in the SV modulator, incorrect duty-cycle values will be calculated resulting in a distorted output voltage. The distortion is most noticeable during low speed operation since the on-state voltage error, which is fixed with respect to motor speed, becomes of comparable size to the commanded converter terminal voltages. By assuming ideal vector locations, the actual converter terminal voltage vector inscribes an approximate hexagonal shape in the $\alpha\beta$ reference

frame since the direction of the on-state voltage error changes 6 times with every electrical cycle, corresponding to the 6 different current polarities experienced over this period.

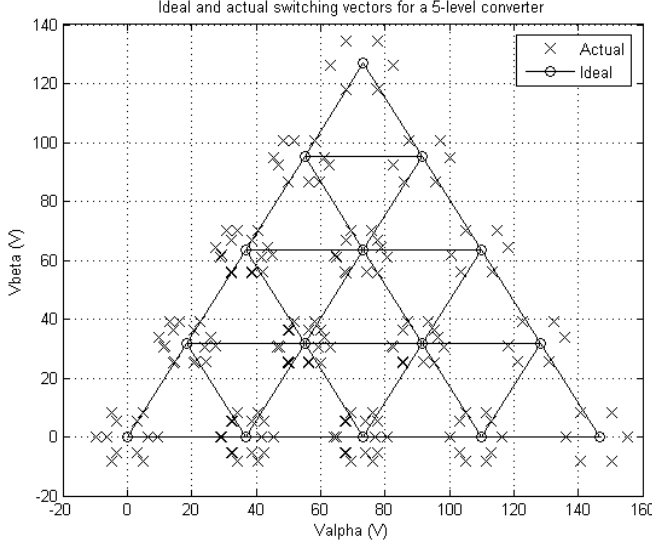


Fig. 2. First sector of SV diagram showing ideal and actual vectors.

It is notable that due to the increased number of devices in the current path, for multilevel converters, the distortion caused by the on-state device voltages is typically greater than for classical 2-level counterparts. For example, a demanded phase terminal voltage of V_{dc} with positive current, results in an actual terminal voltage of a) $V_{dc} - V_{CEon}$ for a 2-level converter b) $V_{dc} - 4V_{CEon}$ for a 5-level converter.

III. DC-LINK VOLTAGE BALANCING

The converter terminal voltage is synthesized within each modulation cycle by switching between the 3 nearest vectors to the reference vector, such that the reference and terminal voltage have the same volt-second equivalent value. The reference vector rotates about the centre of the SV diagram in synchronism with the machine rotor.

A control requirement on the DCC is that the voltages across the series connected DC-link capacitors are balanced and is achieved by switching between redundant vectors that produce the same line-line terminal voltages [17-19]. From Fig. 2 it can be seen that the first sector of the SV diagram for the 5-level case is composed of 16 triangular regions. The ideal switching vectors are sited at the corners of each triangular region. A capacitor balancing scheme is realised by choosing a series of 3 switching vectors that, within each modulation period, minimises:

$$E_b = \frac{1}{2} C \sum_{j=1}^n \Delta V_{ej}^2 \text{ where } \sum_{j=1}^n v_{ej} = V_{DC}, v_{ej} > 0 \quad (2)$$

where [17]:

$$\Delta V_{ej} = V_{ej} - \frac{V_{DC}}{n-1} \quad (3)$$

For (2) and (3), V_{ej} , V_{DC} , C and n are the individual capacitor voltages, the DC-link voltage, the individual capacitances and the number of phase-voltage levels, respectively

The application of redundant vectors for capacitor voltage balancing affects the requirements for dead-time compensation, since, prior to the calculation of the capacitor balancing equations, the actual phase voltages and the size of the phase voltage steps at the switching instances, are unknown. Furthermore, the shape of the phase voltage waveforms may change from one modulation cycle to the next. In addition, any modification to the commanded converter terminal voltages, for compensation, may move the reference vector from one multilevel region to another, dictating a different set of switching vectors are utilised with correspondingly different blanking-time compensation requirements. This interdependence of factors makes it necessary to implement on-state voltage compensation and blanking-time compensation independently.

At this point it should be noted that, more generally, redundant switching vectors may also be used to satisfy criteria other than for capacitor balancing of DCCs. For example, [20] and [21] utilise switching vector redundancies to eliminate common-mode voltages when using a multilevel cascaded H-bridge topology and a 5-level DCC topology, respectively.

IV. PROPOSED ON-STATE COMPENSATION SCHEME

The proposed compensation scheme for the on-state voltage error relies on the fact that, for a known 3-phase current polarity, all the switching vectors share an almost identical offset in the $\alpha\beta$ coordinate frame. By way of example, Fig. 3a shows the ideal and actual switching vectors for the 3-phase current polarity: $I_A > 0; I_B > 0; I_C < 0$. Given that the vector offsets in the stationary $\alpha\beta$ reference frame are similar, it is possible to shift the reference diagram such that the mean average error between the actual vectors and the reference diagram, in the first sextant, is zero (Fig 3b). The offsets are calculated from:

$$V_{\alpha offset} = \frac{1}{m} \sum_{i=1}^m [V_{\alpha error}(i)] \quad (4)$$

$$V_{\beta offset} = \frac{1}{m} \sum_{i=1}^m [V_{\beta error}(i)] \quad (5)$$

where

$$V_{\alpha error}(i) = V_{\alpha actual}(i) - V_{\alpha ideal}(i) \quad (6)$$

$$V_{\beta error}(i) = V_{\beta actual}(i) - V_{\beta ideal}(i) \quad (7)$$

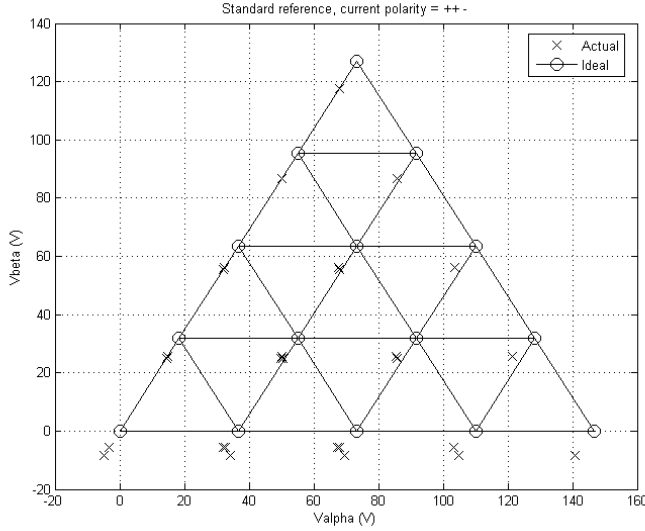
and m is the number of vectors in the first sector.

Shifting the commanded reference vector by an equal amount in the opposing direction to the reference diagram shift, compensates for the shifted switching vectors and removes the error. Removing the error in this way has the

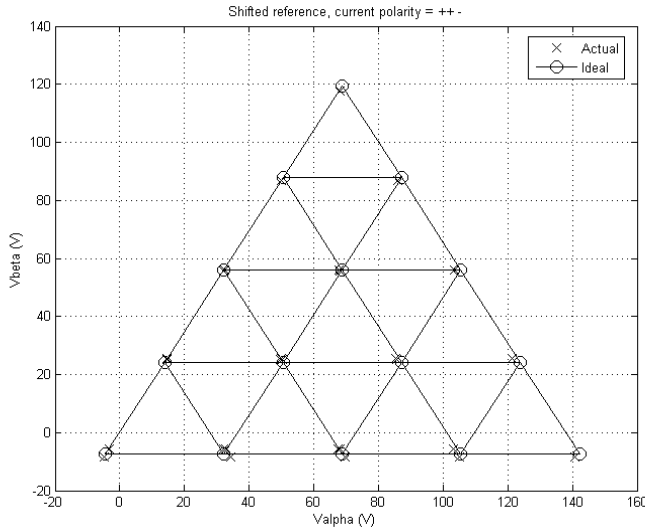
advantage of maintaining the symmetry of the SV diagram, and therefore the simplicity of the region identification and duty-cycle calculation, is maintained. The shifted reference vector is calculated as follows:

$$V\alpha'_{ref} = V\alpha_{ref} - V\alpha_{offset} \quad (8)$$

$$V\beta'_{ref} = V\beta_{ref} - V\beta_{offset} \quad (9)$$



(a)



(b)

Fig. 3. Actual and ideal switching vectors in the sector under current polarity: $I_A > 0; I_B > 0; I_C < 0$ (a) uncompensated, (b) compensated.

The offset values $V\alpha_{offset}$ and $V\beta_{offset}$ are calculated offline as functions of the device voltage drops: V_{CEon} , V_{ff} and V_{fc}

$$V\alpha_{offset} = AV_{CEon} + BV_{FC} + CV_{FF} \quad (10)$$

$$V\beta_{offset} = DV_{CEon} + EV_{FC} + FV_{FF} \quad (11)$$

where parameters A-F are stored in a look-up table for the

various current polarities.

The voltage drops, V_{CEon} , V_{ff} and V_{fc} , are non-linear functions of current, and values are estimated (on-line) with two-straight line approximations for each parameter. The first is a linear resistance that is calculated at relatively low currents, and for higher currents a constant voltage drop with an incremental resistance is used. The dual slope estimation of the device on-state voltages allows the amount of compensation around the zero-crossing region to be reduced, thereby preventing ‘over-compensation’. By way of example, Fig.4. shows V_{CEon} , as a function of current, with two straight lines fitted to the measured curve. The linear resistance approximation is applied in low current region A, while the constant voltage drop + incremental resistance is applied in region B. A flow diagram, for the on-state compensation, is included (Fig.9) in the appendix.

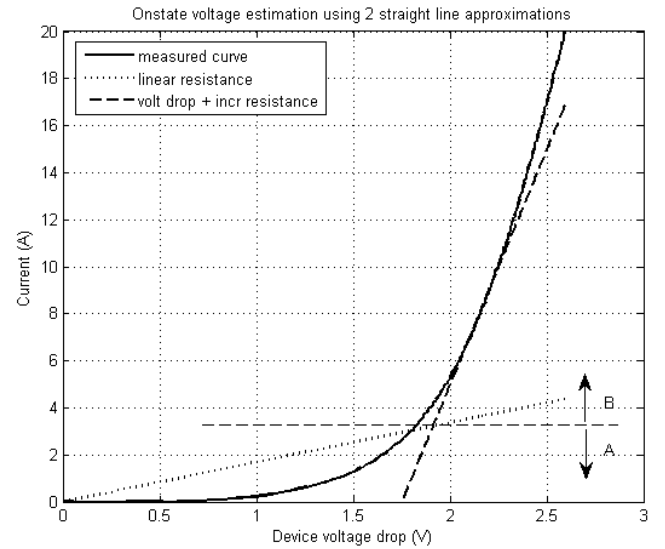


Fig. 4. Measured IGBT on-state voltage, V_{CEon} , and the corresponding approximations

V. BLANKING-TIME COMPENSATION

Fig. 5 shows example waveforms of gate drive signals for a commanded phase voltage step between $V_{dc}/4$ and $3V_{dc}/4$, where blanking-time, t_d , is implemented by delaying the rising edges of the each gate drive signal. For positive current, when the commanded phase voltage steps from $V_{dc}/4$ to $3V_{dc}/4$, IGBTs Q6 and Q7 are turned off while IGBTs Q2 and Q3 are turned on after the blanking-time t_d . During the blanking-time, current continues to flow through D10 and Q4 and only commutates to D14, Q2 and Q3 when Q2 and Q3 have turned on (after the blanking-time), Fig.1. When the commanded voltage returns from $3V_{dc}/4$ to $V_{dc}/4$, Q2 and Q3 are turned off t_d seconds before Q6 and Q7 are turned on. When Q2 and Q3 are turned off, positive current commutates back to D10 and Q4. The net result therefore is an error in the voltage appearing at the converter phase terminal. Averaged over the switching period, T_s , the voltage error is given by:

$$V_{err} = -\frac{V_{dc}td}{2T_s} \quad (12)$$

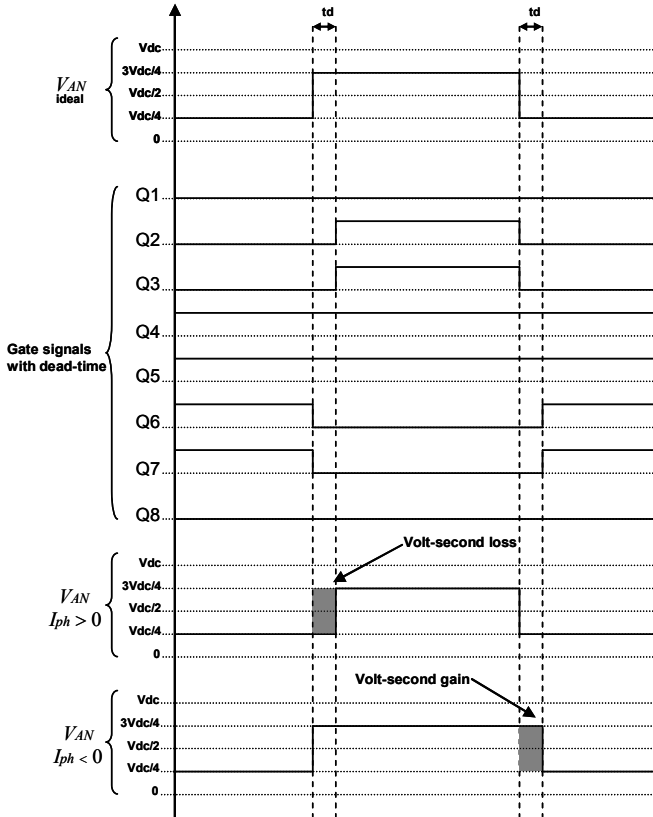


Fig. 5. Example gate drive waveforms and blanking-time effects.

For the negative current case, the state of Q6 and Q7 determine the point at which the current commutates between the Q5, D13 to Q5, Q6, Q7, D9. When the commanded phase voltage drops from $3V_{dc}/4$ to $V_{dc}/4$, the rising edges of Q6 and Q7 are delayed by the blanking-time, and hence, the phase terminal voltage remains at $3V_{dc}/4$ during the blanking period. This results in a voltage error averaged over the switching period:

$$V_{err} = \frac{V_{dc}td}{2T_s} \quad (13)$$

The voltage error for any multilevel step size can therefore be calculated as:

$$V_{err} = -V_{step} \frac{td}{T_s} \text{sgn}(I_{ph}) \quad (14)$$

where V_{step} is the size of the multilevel voltage step and

$$\begin{aligned} \text{sgn}(I_{ph}) &= 1; I_{ph} > 0 \\ \text{sgn}(I_{ph}) &= -1; I_{ph} < 0 \end{aligned} \quad (15)$$

The result (14) shows that the error created by the blanking time is proportional to the size of the voltage step at the switching instant. This voltage step size is determined by the choice of switching sequences made by the capacitor balancing algorithm for a particular modulation period.

To compensate for the blanking-time error voltage, it is proposed to vary the length of the commanded phase voltage

signal prior to the addition of dead-time. The phase current polarity is sampled at the start of the switching cycle and the commanded phase voltage is extended by td seconds if the phase current is positive, or reduced by td seconds if the phase current is negative, where the value of td is known from converter design. By applying this pulse based compensation, the volt-second error, which is dependent on the size of the multilevel step, is therefore compensated.

It should be noted that the on-state compensation and dead time compensation could be applied to modulation schemes other than SVM, for example multilevel Sinusoidal PWM (SPWM). However, the ability of the proposed schemes to compensate for errors resulting from the application of redundant vectors, makes the proposed scheme particularly suited to SVM techniques.

VI. EXPERIMENTAL RESULTS

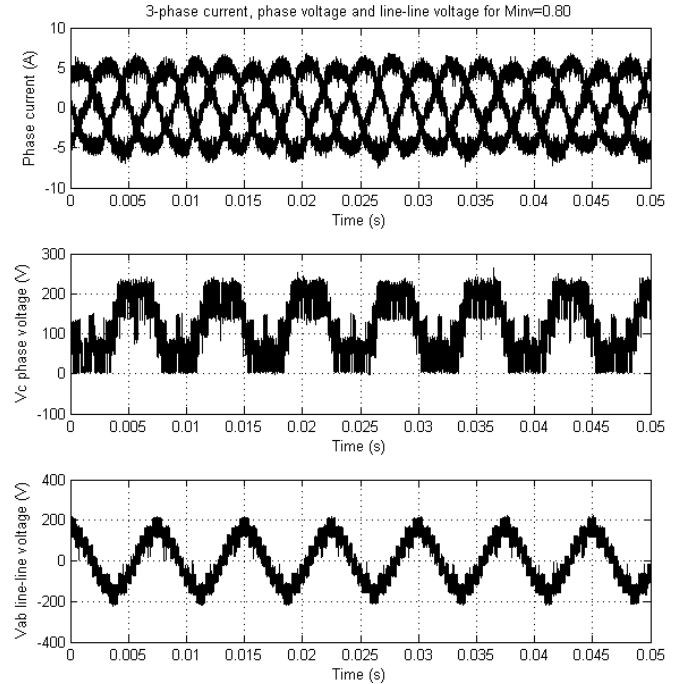


Fig. 6. 3-phase currents, phase and line-line voltage from 5-level inverter

The compensation schemes are applied to a 5-level DCC driving a low-inductance BLAC machine (synchronous inductance $180\mu\text{H}$) operating from a 220V DC-link. Field-orientated control along with the on-state voltage compensation is implemented using a Texas Instruments TMS320C6713 development board, while the gate drive signals and blanking-time compensation are implemented on a Xilinx Spartan 3 development board. For both on-state and dead-time compensation schemes, accurate current polarity detection is crucial for correct compensation since incorrect current polarity determination results in a reinforcement, rather

than a reduction of the dead-time errors. A scheme detailed in [9], which low-pass-filters the currents in the rotating dq axis prior to conversion into the stationary $\alpha\beta$ axis for polarity determination, is therefore employed.

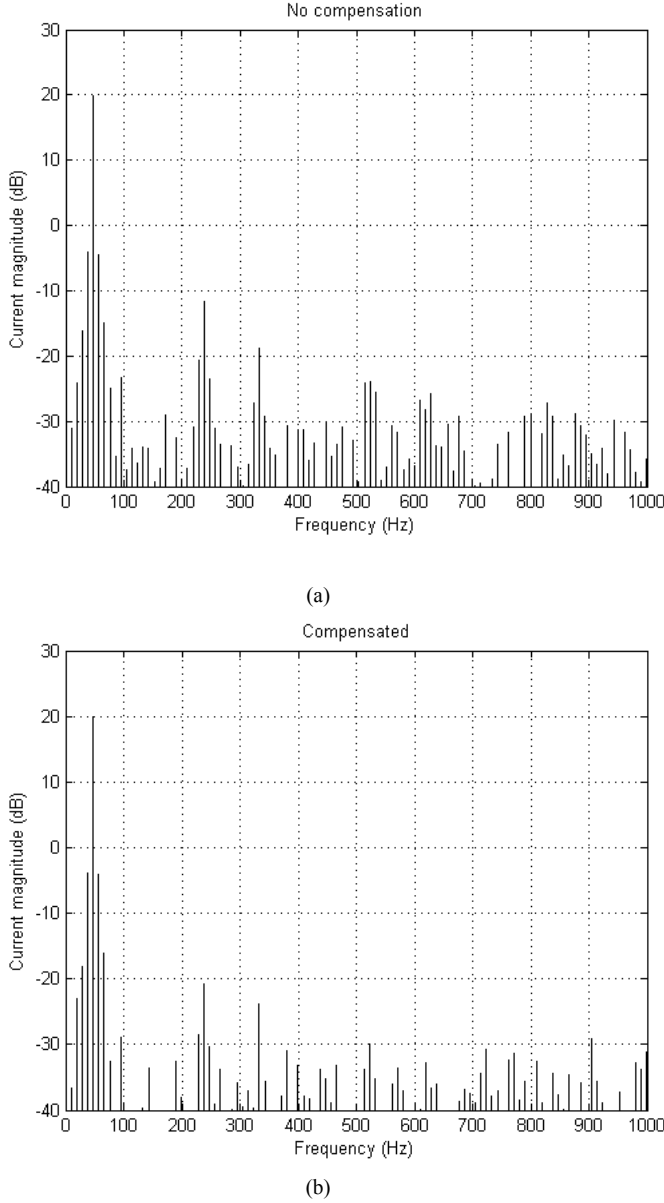


Fig. 7. FFT of phase current, (a) no compensation, (b) blanking-time and on-state voltage compensation.

Fig. 6 shows example 3-phase currents, phase voltage and line-line voltage from the 5-level inverter operating at an inverter modulation index $m_{inv} = 0.8$.

Figs. 7 a-b compare the low frequency phase current harmonics between the non-compensated and compensated cases (both blanking-time and on-state voltage drop compensation). The first notable harmonic is the 5th at around 240Hz with the compensated scheme reducing this harmonic by 9.1dB. Reductions in the 7th and 11th harmonics are also shown to be 5.0dB and 5.9dB, respectively. Figs. 8 a-b show the 3 phase currents, converted into the $\alpha\beta$ frame and then

plotted as a locus plot for the uncompensated and compensated cases, respectively. The reduction in low frequency harmonics in the compensated case is clearly shown with the uncompensated case appearing more hexagonal rather than the circular form of the compensated case.

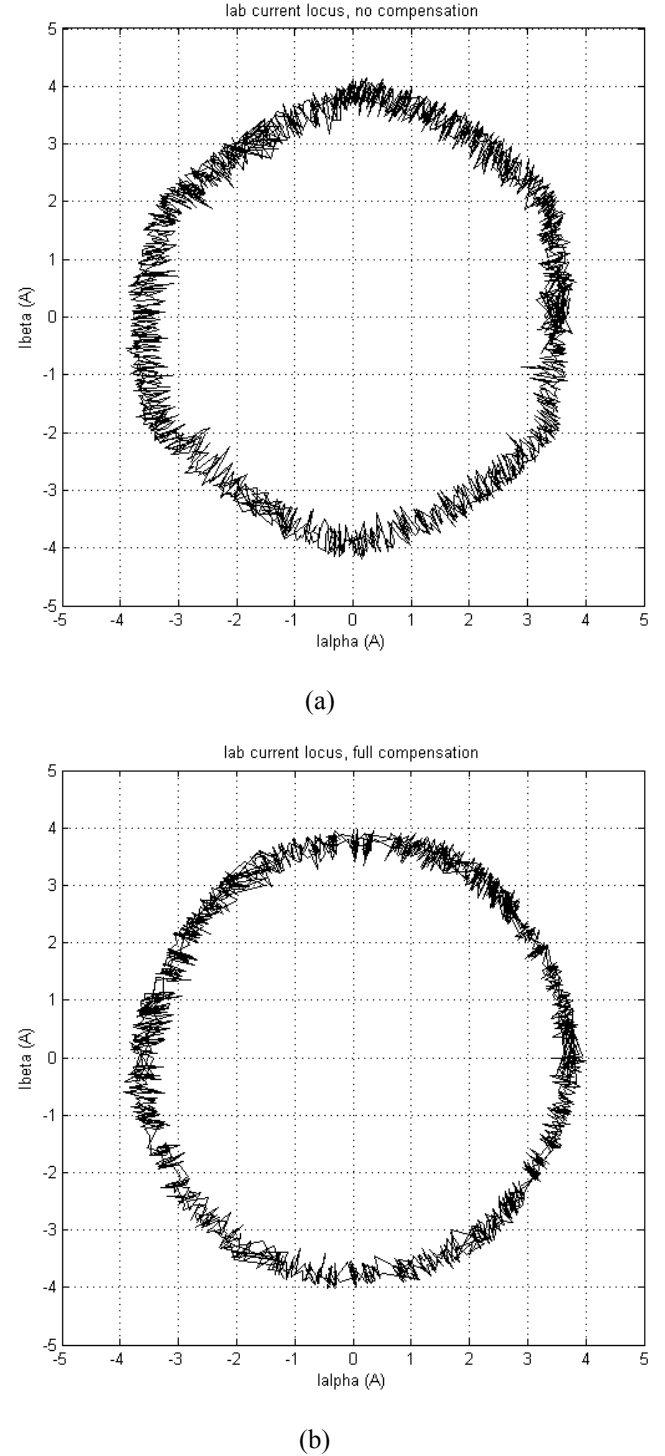


Fig. 8. $\alpha\beta$ current locus, (a) no compensation, (b) blanking-time and on-state voltage compensation.

Harmonics in the current waveform result in torque pulsations from the permanent magnet machine and so

reducing these harmonics, with the proposed scheme, provides for smoother torque production. Furthermore, system efficiency will increase as the harmonics are responsible for extra power losses in the machine and power converter.

VII. CONCLUSION

The paper proposes a simple solution to minimise the error created by on-state device voltage drops while also compensating for the blanking-time inserted to prevent shoot-through, for multilevel DCCs, operating with redundant vector selection. To-date, the additional voltage drops and complexity of compensating for dead-time effects, have not been considered in previous literature.

Experimental results, gathered from a prototype 5-level converter, have shown that the compensation scheme reduces the low frequency harmonics when compared to the uncompensated case. The improvement in current quality is readily apparent from a locus plot of the phase currents in the $\alpha\beta$ reference frame. Low frequency harmonics are shown to create a hexagonal locus for the uncompensated case, while the compensated case shows a circular locus, thereby indicating higher quality sinusoidal phase currents. Furthermore, a harmonic analysis has shown reductions in the 5th, 7th and 11th harmonics by 9.1dB, 5.0dB and 5.9dB, respectively. Ultimately, the mitigation of low frequency harmonics facilitates stable motor torque production with reduced torque pulsations and lower power losses.

VIII. APPENDIX

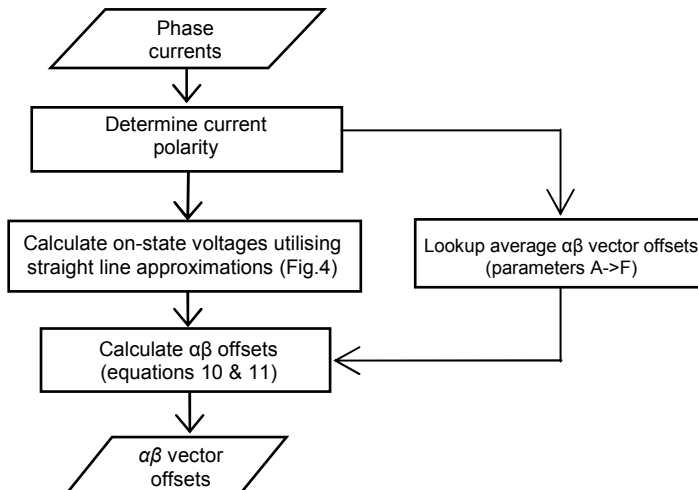


Fig. 9. On-state voltage compensation flow diagram

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